IN THE CLAIMS:

Please amend the claims as follows:

1-9. (Canceled)

10. (Currently Amended) A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

a plurality of input/output cells including circuit elements formed so as to be peripherally arranged on a surface of the semiconductor chip, and

a plurality of electrode pads formed on associated ones of the input/output cells;

the electrode pads are configured in a zigzag pad arrangement so as to form inner and outer pad arrays; and

a predetermined area near a corner on the semiconductor chip surface is designated as a pad-disposition restriction area, within which disposing and usage of one or ones of the electrode pads that are bump-bonded to an interconnect pattern formed on a surface of the carrier are restricted, [~~The device of claim 1,~~]

wherein in the pad-disposition restriction area, the inner pad array is individually bump-bonded to the interconnect pattern on the carrier surface, and at least two of the electrode pads are short-circuited to each other inside the carrier.

11. (Original) The device of claim 10, wherein the electrode pads that are short-circuited to each other inside the carrier are connected via the carrier to a power supply or to ground.

12. (Original) The device of claim 10, wherein of the input/output cells, those corresponding to the electrode pads that are short-circuited to each other inside the carrier function as a single high-drive-current capability cell.

13. (Original) The device of claim 10, wherein of the input/output cells, those corresponding to the electrode pads that are short-circuited to each other inside the carrier function as a single low-impedance cell.

14. (New) The semiconductor device of claim 10, wherein each of the electrode pads has a tenon-like conformation in plan view, and includes a narrow probing portion and a wide bonding portion which is bump-bonded to a interconnect pattern on the carrier.

15. (New) A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

a plurality of input/output (I/O) cells each including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including first and second I/O groups each including at least two I/O cells, wherein

the first I/O group includes at least two first I/O cells each having an inner electrode pad as the electrode pad and at least two second I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two first and second I/O cells included in the first I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the second I/O group is formed in a region between a corner region of the semiconductor chip and the first I/O group, and includes at least two third I/O cells each having an outer

electrode pad as the electrode pad, and said electrode pads included in the second I/O group are configured to form only outer pad array.

16. (New) The semiconductor device of claim 15, wherein each of a plurality of electrode pads of the plurality of I/O cells has a tenon-like conformation in plan view, and includes a narrow probing portion and a wide bonding portion which is bump-bonded to a interconnect pattern on the carrier.

17. (New) The semiconductor device of claim 15, wherein the second I/O group further includes a plurality of cells each having no electrode pad and each of the plurality of cells is formed between any two adjacent ones of the at least two third I/O cells included in the second I/O group.

18. (New) The semiconductor device of claim 15, wherein a pitch of each two adjacent ones of at least two outer electrode pads of the at least two third I/O cells included in the second I/O group is smaller than a pitch of each two adjacent ones of at least two outer electrode pads of the at least two second I/O cells included in the first I/O group.

19. (New) The semiconductor device of claim 15, wherein the semiconductor chip further includes a corner cell formed in the corner region of the semiconductor chip and the second I/O group is formed to be adjacent to the corner cell.

20. (New) A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

a plurality of I/O cells each including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including first and second I/O groups each including at least two I/O cells, wherein

the first I/O group includes at least two first I/O cells each having an inner electrode pad as the electrode pad and at least two second I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two first and second I/O cells included in the first I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the second I/O group is formed in a region between a corner region of the semiconductor chip and the first I/O group, and includes at least two third I/O cells each having an outer electrode pad as the electrode pad and at least two fourth I/O cells each having an inner electrode pad as the electrode pad, and a plurality of electrode pads of the at least two third and fourth I/O cells included in the second I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays,

wherein each inner electrode pad of each of the at least two fourth I/O cells included in the second I/O group is smaller than each inner electrode pad of each of the at least two first I/O cells included in the first I/O group.

21. (New) The semiconductor device of claim 20, wherein the carrier includes a first plurality of interconnect patterns each electrically connected to each inner electrode pad of the at least two first I/O cells, a second plurality of interconnect patterns each electrically connected to each outer electrode pad of the at least two second I/O cells, and a third plurality of interconnect patterns each electrically connected to each outer electrode pad of the at least two third I/O cells and does not include any interconnect pattern electrically connected to any of the at least two inner electrode pads of the at least two fourth I/O cells.

22. (New) The semiconductor device of claim 20, wherein each of a plurality of electrode pads of the plurality of I/O cells has a tenon-like conformation in plan view, and

includes a narrow probing portion and a wide bonding portion which is bump-bonded to a interconnect pattern on the carrier.

23. (New) The semiconductor device of claim 20, wherein the semiconductor chip further includes a corner cell formed in the corner region of the semiconductor chip and the second I/O group is formed to be adjacent to the corner cell.

24. (New) A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

a plurality of I/O cells each including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including first and second I/O groups each including at least two I/O cells, wherein

the first I/O group includes at least two first I/O cells each having an inner electrode pad as the electrode pad and at least two second I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two first and second I/O cells included in the first I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the second I/O group is formed in a region between a corner region of the semiconductor chip and the first I/O group, and includes at least two third I/O cells each having an outer electrode pad as the electrode pad and at least two fourth I/O cells each having an inner electrode pad as the electrode pad, and a plurality of electrode pads of the at least two third and fourth I/O cells included in the second I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays,

wherein the carrier includes:

a first plurality of interconnect patterns each electrically connected to each inner electrode pad of the at least two first I/O cells;

a second plurality of interconnect patterns each electrically connected to each outer electrode pad of the at least two second I/O cells;

a third plurality of interconnect patterns each electrically connected to each outer electrode pad of the at least two third I/O cells; and

a fourth interconnect pattern electrically connected to an inner electrode pad of a corresponding one of the at least two fourth I/O cells,

wherein the carrier does not include any interconnect pattern electrically connected to an another inner electrode pad of a corresponding one of the at least two fourth I/O cells.

25. (New) The semiconductor device of claim 24, wherein each of a plurality of electrode pads of the plurality of I/O cells has a tenon-like conformation in plan view, and includes a narrow probing portion and a wide bonding portion which is bump-bonded to a interconnect pattern on the carrier.

26. (New) The semiconductor device of claim 24, wherein the semiconductor chip further includes a corner cell formed in the corner region of the semiconductor chip and the second I/O group is formed to be adjacent to the corner cell.

27. (New) A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

a plurality of I/O cells each including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including first and second I/O groups each including at least two I/O cells, wherein

the first I/O group includes at least two first I/O cells each having an inner electrode pad as the electrode pad and at least two second I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two first and second I/O cells included in the first I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the second I/O group is formed in a region between a corner region of the semiconductor chip and the first I/O group, and includes at least two third I/O cells each having an outer electrode pad as the electrode pad and at least two fourth I/O cells each having an inner electrode pad as the electrode pad, and a plurality of electrode pads of the at least two third and fourth I/O cells included in the second I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays,

wherein the carrier includes an interconnect pattern electrically connected to at least two of the at least two inner electrode pads of the at least two fourth I/O cells.

28. (New) The semiconductor device of claim 27, wherein each of a plurality of electrode pads of the plurality of I/O cells has a tenon-like conformation in plan view, and includes a narrow probing portion and a wide bonding portion which is bump-bonded to a interconnect pattern on the carrier.

29. (New) The semiconductor device of claim 27, wherein the semiconductor chip further includes a corner cell formed in the corner region of the semiconductor chip and the second I/O group is formed to be adjacent to the corner cell.

30. (New) A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

a first plurality of I/O cells formed along a first side of the semiconductor chip and each including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including first and second I/O groups each including at least two I/O cells, wherein

the first I/O group includes at least two first I/O cells each having an inner electrode pad as the electrode pad and at least two second I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two first and second I/O cells included in the first I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the second I/O group is formed in a region between a corner region of the semiconductor chip and the first I/O group, and includes at least two third I/O cells each having an outer electrode pad as the electrode pad and at least two fourth I/O cells each having an inner electrode pad as the electrode pad, and a plurality of electrode pads of the at least two third and fourth I/O cells included in the second I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays; and

a second plurality of I/O cells formed along a second side of the semiconductor chip, the first and second sides of the semiconductor chip both sharing with the corner region of the semiconductor chip and each of the second plurality of I/O cells including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including third and fourth I/O groups each including at least two I/O cells, wherein

the third I/O group includes at least two fifth I/O cells each having an inner electrode pad as the electrode pad and at least two sixth I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two fifth and sixth I/O cells

included in the third I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the fourth I/O group is formed in a region between the corner region of the semiconductor chip and the third I/O group, and includes at least two seventh I/O cells each having an outer electrode pad as the electrode pad and at least two eighth I/O cells each having an inner electrode pad as the electrode pad, and a plurality of electrode pads of the at least two seventh and eighth I/O cells included in the fourth I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays,

wherein the carrier includes an interconnect pattern electrically connected to both an inner electrode pad of the at least two inner electrode pads of the at least two fourth I/O cells and an inner electrode pad of the at least two inner electrode pads of the at least two eighth I/O cells.

31. (New) The semiconductor device of claim 30, wherein each of a plurality of electrode pads of the first plurality of I/O cells and the second plurality of I/O cells has a tenon-like conformation in plan view, and includes a narrow probing portion and a wide bonding portion which is bump-bonded to a interconnect pattern on the carrier.

32. (New) The semiconductor device of claim 30, wherein the semiconductor chip further includes a corner cell formed in the corner region of the semiconductor chip and each of the second and fourth I/O groups is formed to be adjacent to the corner cell.

33. (New) A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

a first plurality of I/O cells formed along a first side of the semiconductor chip and each including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including first and second I/O groups each including at least two I/O cells, wherein

the first I/O group includes at least two first I/O cells each having an inner electrode pad as the electrode pad and at least two second I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two first and second I/O cells included in the first I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the second I/O group is formed in a region between a corner region of the semiconductor chip and the first I/O group, and includes at least two third I/O cells each having an outer electrode pad as the electrode pad, and said electrode pads included in the second I/O group are configured to form only outer pad array; and

a second plurality of I/O cells formed along a second side of the semiconductor chip, the first and second sides of the semiconductor chip both sharing with the corner region of the semiconductor chip and each of the second plurality of I/O cells including a circuit element and an electrode pad formed on the circuit element, the plurality of I/O cells including third and fourth I/O groups each including at least two I/O cells, wherein

the third I/O group includes at least two fourth I/O cells each having an inner electrode pad as the electrode pad and at least two fifth I/O cells each having an outer electrode pad as the electrode pad, and a plurality of electrode pads of the at least two fourth and fifth I/O cells included in the third I/O group are configured in a zigzag pad arrangement so as to form inner and outer pad arrays, and

the fourth I/O group is formed in a region between the corner region of the semiconductor chip and the third I/O group, and includes at least two sixth I/O cells each having an outer electrode pad as the electrode pad, and said electrode pads included in the fourth I/O group are configured to form only outer pad array.

34. (New) The semiconductor device of claim 33, wherein each of a plurality of electrode pads of the plurality of I/O cells has a tenon-like conformation in plan view, and includes a narrow probing portion and a wide bonding portion which is bump-bonded to a interconnect pattern on the carrier.

35. (New) The semiconductor device of claim 33, wherein the semiconductor chip further includes a corner cell formed in the corner region of the semiconductor chip and each of the second and fourth I/O groups is formed to be adjacent to the corner cell.

36. (New) The semiconductor device of claim 33, wherein the second I/O group further includes a first plurality of cells each having no electrode pad and each of the first plurality of cells is formed between any two adjacent ones of the at least two third I/O cells included in the second I/O group and the fourth I/O group further includes a second plurality of cells each having no electrode pad and each of the second plurality of cells is formed between any two adjacent ones of the at least two sixth I/O cells included in the fourth I/O group.